AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0012] with the following context:

"As described, the process for forming the N doped regions 76 is performed after forming the composite dielectric layer 62 according to the conventional method. In other words, the composite dielectric layer 62 between any two adjacent sacrificial spacers 72 must be removed before forming the N doped regions 76. In addition, the blocking film 78 has to be formed before forming the word lines 80, or alternatively another silicon oxide layer (not shown) has to be formed after removing the sacrificial spacers [[76]] 72 to avoid short circuits between the word lines 80 and the N doped regions (buried bit lines) 76. It is appreciated that even though the short circuit problem is avoided by forming the blocking film 78, other factors, such as the incompletion of the composite dielectric layer 62, the remaining etching stress, and the etching infirmity, may cause damages to the SPVG SONOS memory. For example, a higher voltage difference between the word lines and the buried bit lines may be necessary when performing the erasing operation, or a current leakage problem may occur. This leads to tunneling between the word lines and the buried bit lines, and reduces the reliability of SPVG SONOS memory."